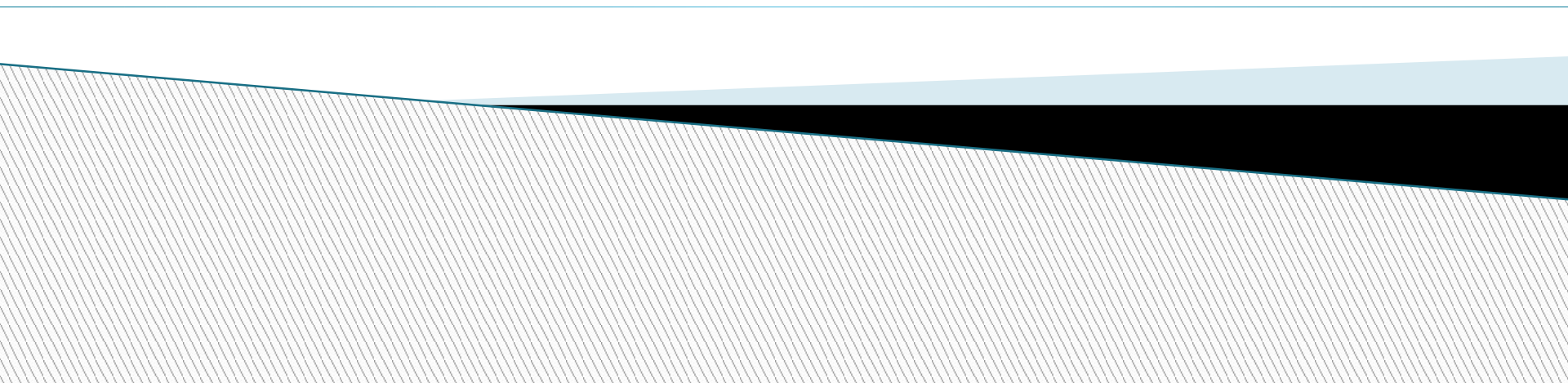


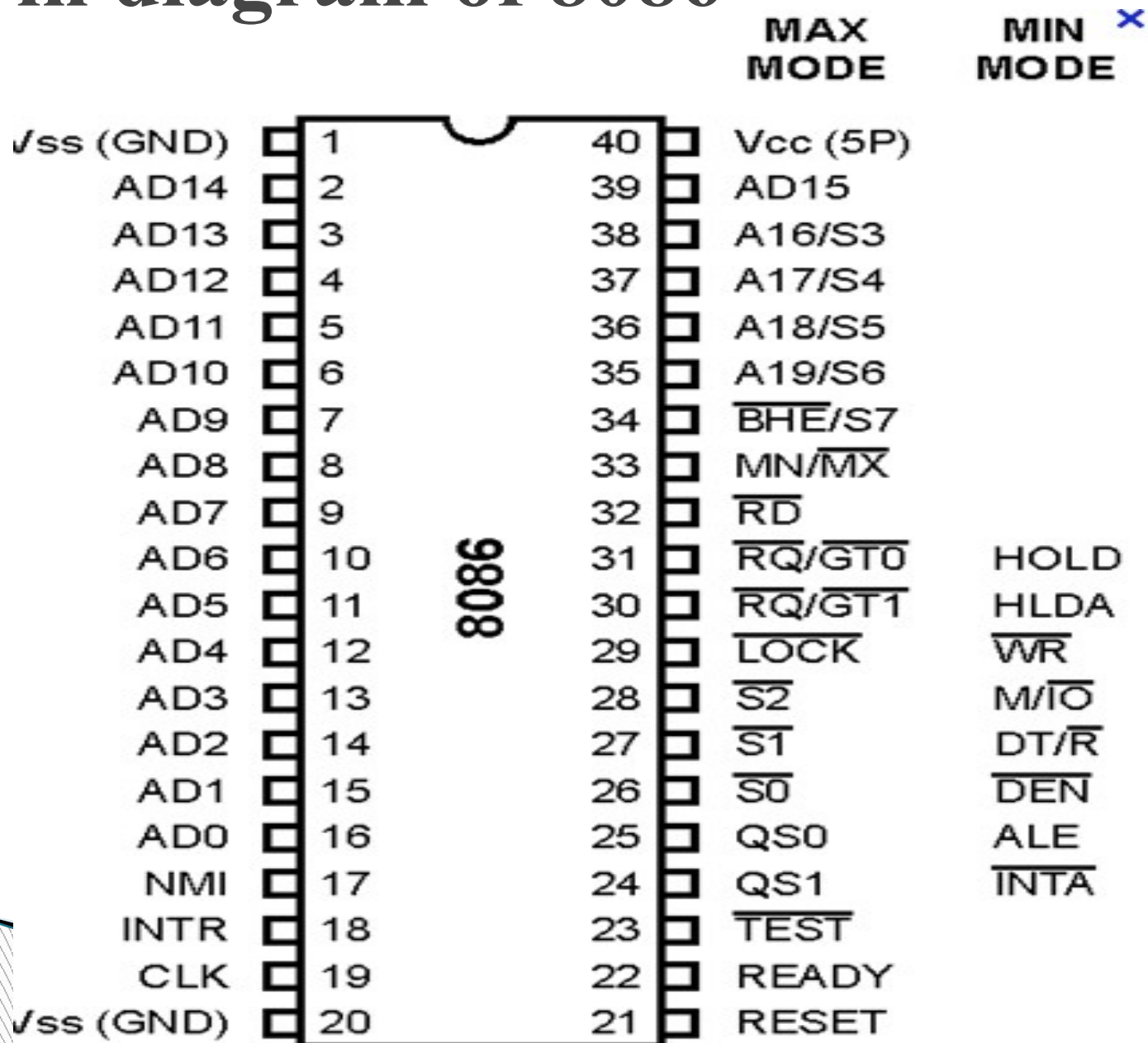
Pin Diagram Of 8086 Microprocessor



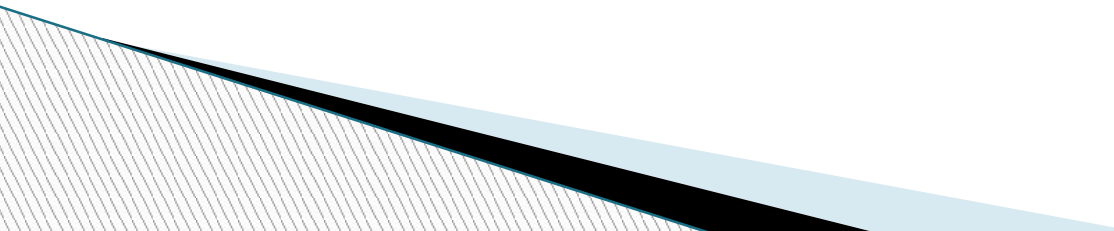
Introduction

- ▶ Pin diagram is shows all the signal pins used by the microprocessor and the sequence of the signals and their connections. 8085 microprocessor is a 40 pin IC which operate on 5volt power supply.

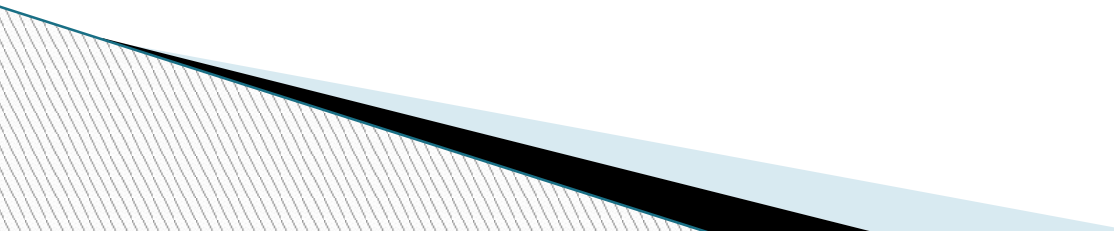
Pin diagram of 8086



Pin Description

- ▶ The Microprocessor 8086 is a 16-bit CPU available in different clock rates and packaged in a 40 pin DIP or plastic package.
 - ▶ The 8086 **operates in single processor or multiprocessor** configuration to achieve high performance. The pins serve a particular function in minimum mode (single processor mode) and other function in maximum mode configuration (multiprocessor mode).
- 

continue

- ▶ The 8086 signals can be categorized in three groups. The first are the signal having **common functions** in **minimum as well as maximum mode**.
 - ▶ The second are the signals which have special functions for **minimum mode**
 - ▶ The third are the signals having special functions for **maximum mode**.
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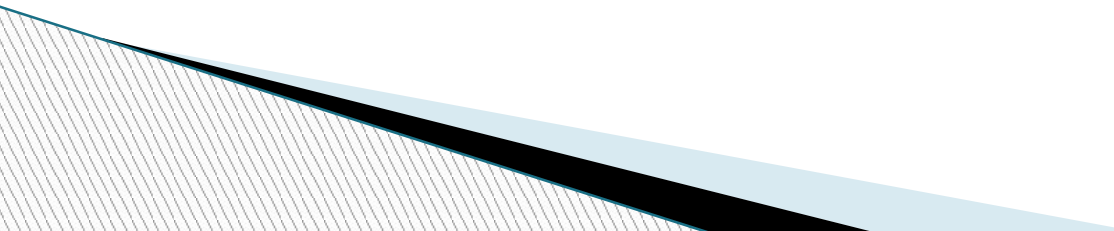
AD15-AD0

- ▶ The following signal descriptions are common for both modes.
- ▶ **AD15-AD0** : These are the time multiplexed memory I/O address and data lines.
 - Address remains on the lines during T1 state, while the data is available on the data bus during T2, T3, Tw and T4. These lines are active high and float to a tristate during interrupt acknowledge and local bus hold acknowledge cycles.

A19-A16

- ▶ **A19/S6, A18/S5, A17/S4, A16/S3** : These are the time multiplexed address and status lines. During T1 these are the most significant address lines for memory operations.
- ▶ During I/O operations, these lines are low.
- ▶ During memory or I/O operations, status information is available on those lines for T2, T3, Tw and T4.
- ▶ The status of the interrupt enable flag bit is updated at the beginning of each clock cycle.

Continue.

- ▶ The **S4 and S3** combinely indicate **which segment register is presently being used** for memory accesses as in below fig.
 - ▶ These lines float to tri-state off during the local bus hold acknowledge. The status line S6 is always low.
 - ▶ The address bit are separated from the status bit using latches controlled by the ALE signal
- 

Segment access

S ₄	S ₃	Indication
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data
0	0	Whole word
0	1	Upper byte from or to even address
1	0	Lower byte from or to even address

BHE/S7

- ▶ **BHE/S7** : The bus high enable is used to indicate the transfer of data over the higher order (D15-D8) data bus . It goes low for the data transfer over D15-D8 and is used to derive chip selects of odd address memory bank or peripherals. BHE is low during T1 for read, write and interrupt acknowledge cycles, whenever a byte is to be transferred on higher byte of data bus. The status information is available during T2, T3 and T4. The signal is active low and tristated during hold. It is low during T1 for the first pulse of the interrupt acknowledge cycle.

Rd, READY

- ▶ **RD – Read** : This signal on low indicates the peripheral that the processor is performing memory or I/O read operation. RD is active low and shows the state for T2, T3, Tw of any read cycle. The signal remains tristated during the hold acknowledge.
- ▶ **READY** : This is the acknowledgement from the slow device or memory that they have completed the data transfer. The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the 8086. the signal is active high.

INTR

- ▶ **INTR-Interrupt Request** : This is a triggered input. This is **sampled during the last clock cycles of each instruction** to determine the availability of the request. If any interrupt request **is pending**, the processor enters the **interrupt acknowledge cycle**. This can be internally masked by resulting the interrupt enable flag. This signal is active high and internally synchronized.

TEST,CLK

- ▶ **TEST** : This input is examined by a ‘WAIT’ instruction. **If the TEST pin goes low, execution will continue, else the processor remains in an idle state.** The input is synchronized internally during each clock cycle on leading edge of clock.
- ▶ **CLK- Clock Input** : The clock input provides the basic timing for processor operation and bus control activity. Its an asymmetric square wave with 33% duty cycle.

Scope

Scope of research can be in the following fields such as

- A) decrease the size of microprocessor.
- B) decrease the power requirement.
- C) increase the feature of microprocessor.
- D) change the manufacturing technology.
- E) change the material which is used.
- F) decrease the weight of the IC.
- G) increase/decrease of Fan in and out.